THEORY & OBJECTIVE

POWER ELECTRONICS

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CONTENTS

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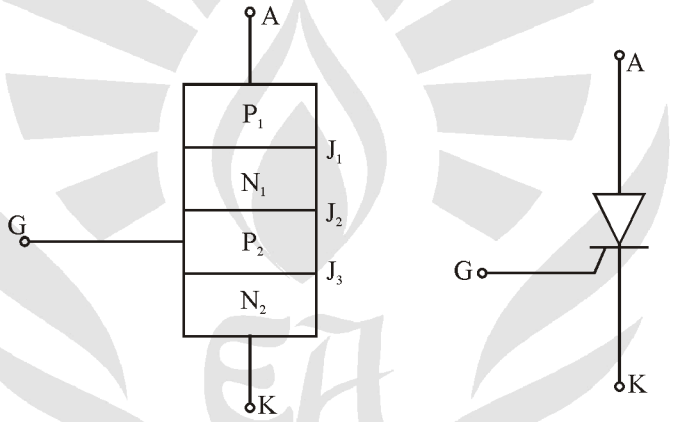
SCR

THEORY

2.1 *INTRODUCTION*

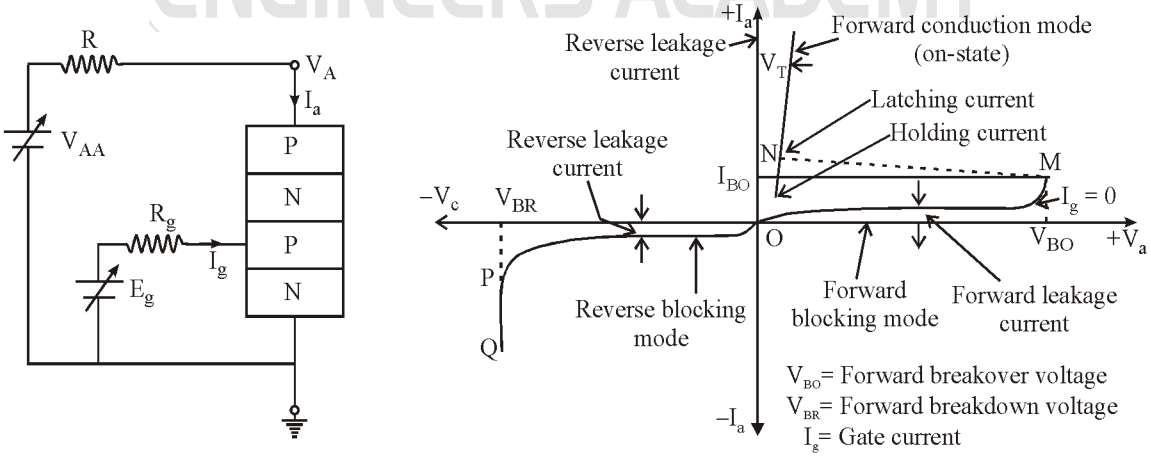
Thyristor (SCR) is 4 layer, 3 p-n junction, charge controlled semi conductor device. It has three terminals called Gate(G), Anode (A) and Cathode (K).Inner two layers of SCR are lightly doped so that the strength of junction J_2 is more than the strength of junctions of J_1 and J_3. SCRs are used up to 3000 A and Voltage up to 10 kV.



Layer Diagram *Symbol*

Outer layers are heavily doped as Compared to inner layers.

2.2 *I-V CHARACTERISTICS*



2.2.1 Forward Blocking Mode :

In this mode of operation SCR is applied with positive anode voltage. The junctions J_1 and J_3 are in forward bias and J_2 is reverse bias and the device is in off state. The device remains in this mode until the anode voltage reaches a critical value called forward break over voltage (V_{FBO}).

2.2.2 Forward Conducting Mode :

When the anode voltage is greater than the forward break over voltage then avalanche break down occurs at Junction J_2 and the device starts conducting.In forward conduction mode SCR behaves like a closed switch. SCR start conducting only if the current through the device is greater than a minimum current called latching current during the turning ON process.

3.2.3 Reverse Blocking State :

When the anode voltage is negative, the junctions J_1 and J_3 are in reverse bias and junction J_2 is in forward bias, the device is in off state and this region of characteristic curve is called reverse blocking state. When the reverse voltage becomes more than V_{RBO} then avalanche break down occurs at reverse bias junctions J_1 and J_3 and the device start conducting in reverse direction.

2.2.4 Latching Current :

It is the minimum anode current required to turn on the SCR during turning on process. Latch current is related to turn on process where as the holding current is related to turn off process because when the junction J_2 breaks down then large number of carriers are generated. So, the large current starts flowing, this current is latch current.

2.2.5 Holding Current :

When the device is already in conducting state and if the anode current is reduced below a minimum level, the device gets turn off. This minimum current required to turn off device is called holding current. The holding current is therefore related to the turn off process. The holding current is always less than the latch current because current continues to flow even below latch current due to charges stored in layers.

Now to turn off the device the current has to be reduced till all the carriers are after re-combination anode current will be less than holding current.

Note: $\boxed{V_{RBO} > V_{FBO}}$ $\quad I_L > I_H$ $\qquad \boxed{\frac{I_L}{I_H} \approx 3}$

2.2.6 Forward Break Over Voltage :

It is the critical voltage required for breakdown of junction J_2 under forward biased condition. It is minimum voltage to be applied across the device for turn ON the device cut out gate signal.

When anode voltage becomes equal to forward break over voltage the junction J_2 breaks down due to Avalanche multiplication and the device start conducting.The forward break over voltage can be reduced by applying a positive pulse at gate terminals. When the gate current increases, the forward break over voltage decreases.

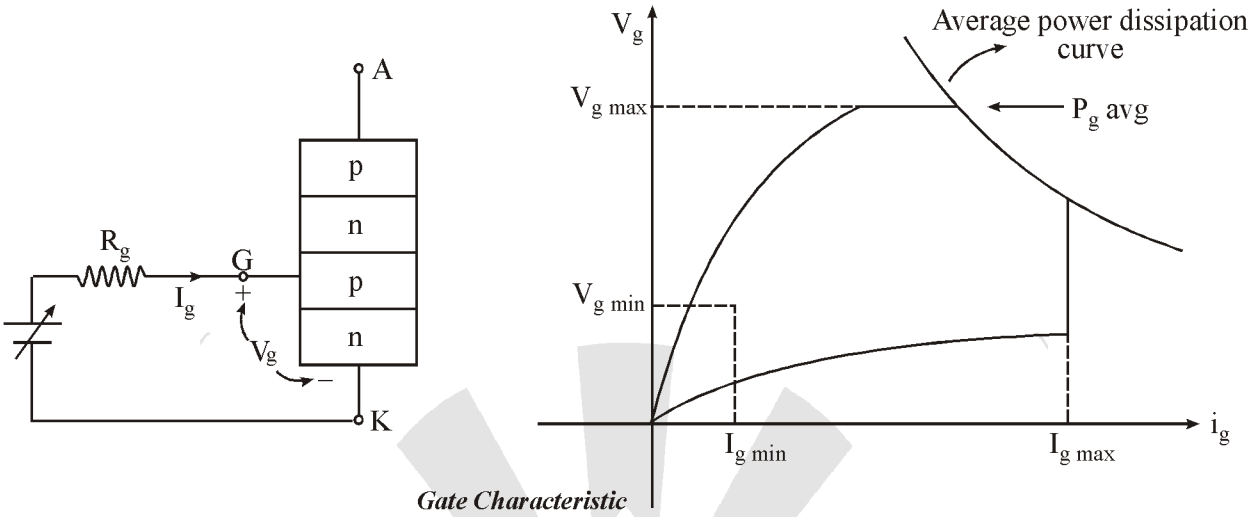
2.2.7 Zener Break Down :

Depends on voltage and dopping level. both layers must be highly dopped, small voltage is required for break down. It is electrostatic breakdown.

2.2.8 Avalanche Break Down :

It occurs due to thermal effect or temperature. It occurs in lightly doped semiconductor junctions.

2.2.9 Gate Characteristic :



Gate Characteristic

Where I_{gmax} = Maximum gate current allowed

V_{gmax} = Maximum gate voltage

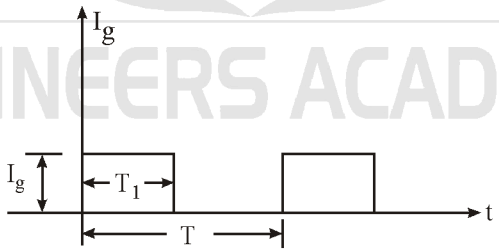
V_{gmin} = Minimum gate voltage

I_{gmin} = Minimum gate current

V_{gmin} and I_{gmin} are decided by satisfactory turning off of the device.

For the satisfactory turning on, the operating point of gate characteristic should always lie nearest to P_{avg} curve.

The turn on time of the thyristor can be reduced by increasing the amplitude of gate current and power dissipation can be reduced by reducing the period of gate pulse in pulse triggering the thyristor remains in on state even if gate current is reduced to zero once it turned ON by pulse triggering.

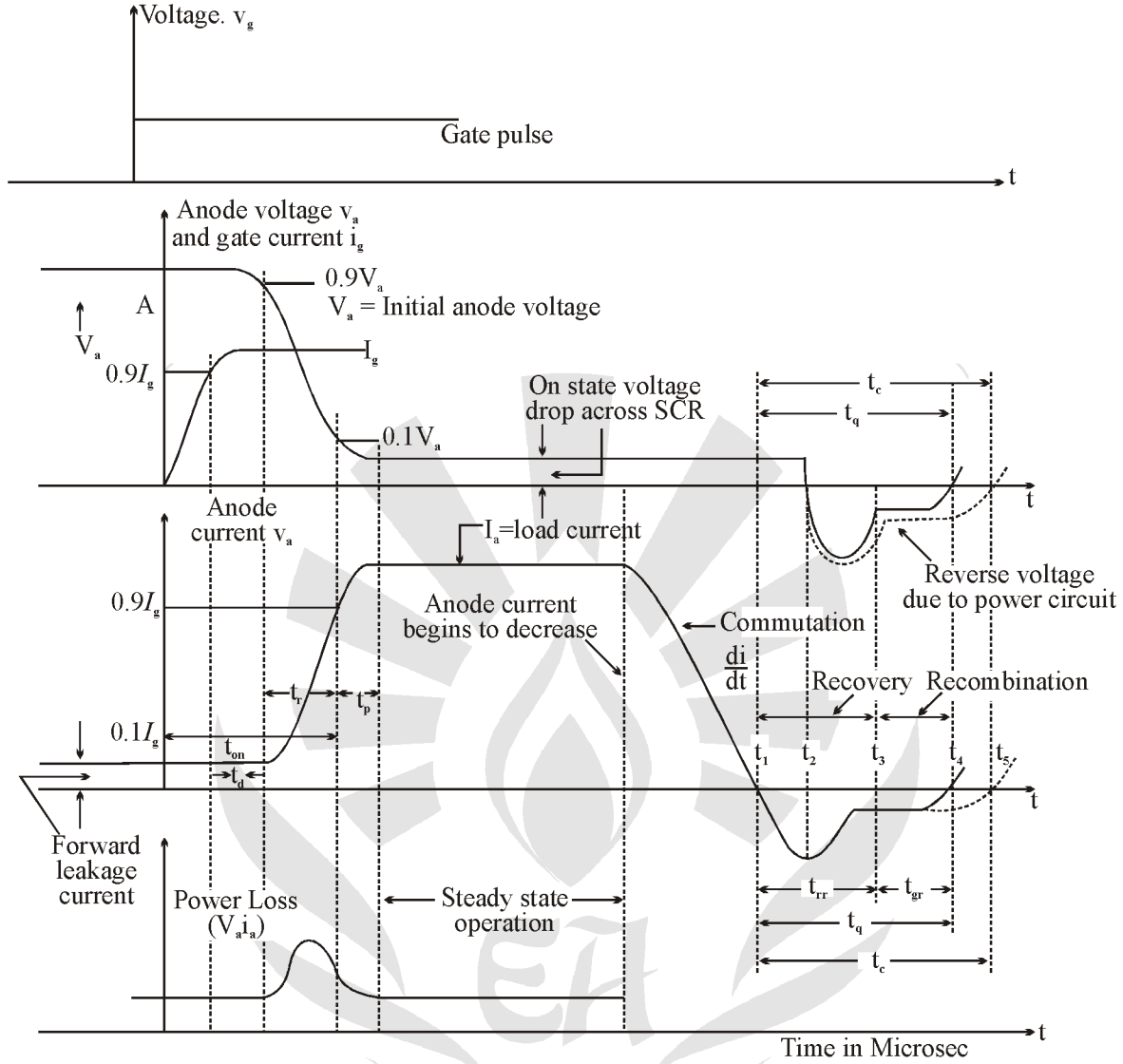


$$d = \text{duty cycle} = \frac{T_1}{T}$$

$$\frac{I_{g\,avg}}{\delta} \le I_{gm}$$ (more power dissipation in gate)

$\delta = f\ T_1$ There f is the frequency of firing or triggering pulse

2.3 *SWITCHING CHARACTERISTICS OF SCR*



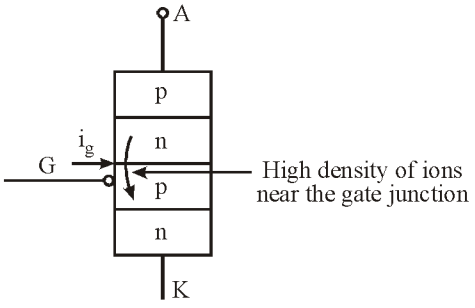
SCR Voltage and current waveforms during turn-on and turn-off processes.

2.3.1 *TURN ON TIME*

Delay time (t_d) : Time taken to rise the i_a from 0% to 10% of full load current, when the gate pulse is applied.

Rise time (t_r) : Time taken to rise the i_a from 10% to 90% of full load current.

Spread time (t_p) : Time taken to rise the i_a from 90% to full load current or it is time taken to spread the conducting channel (conduction) through out the junction.Once the device has turn on.



2.3.2 TURN OFF TIME

t_{rr} = reverse recovery time

t_{gr} = gate recovery time

t_q = turn off time

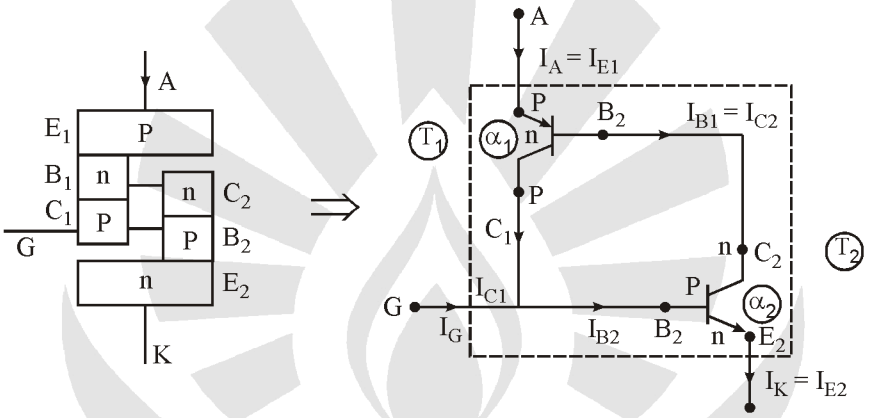
$t_q = t_{rr} + t_{gr}$

Turn off time is the time taken by the SCR to regain its forward blocking capability after the anode current is reduced to zero.

Losses in the SCR are maximum during turning on and turning off process.

Note : *for the proper operation of SCR the circuit turn off time must be greater than the thyristor turn off time.*

2.4 *TWO TRANSISTOR MODEL*



When Devices is conducting then :

$$I_{C1} = \alpha_1 I_{E1} + I_{CBO1}$$

$$\Rightarrow \quad I_{C1} = \alpha_1 I_A + I_{CBO1} \qquad \ldots(i)$$

$$I_{C2} = \alpha_2 I_{E2} + I_{CBO2}$$

$$\Rightarrow \quad I_{C2} = \alpha_2 I_k + I_{CBO2} = I_{B1} \qquad \ldots(ii)$$

$$I_{B1} + I_{C1} = I_{E1}$$

$$I_{B1} = I_{E1} - I_{C1} \qquad \text{[From (ii)]}$$

$$I_{B1} = I_A - [\alpha_2 I_A + I_{CBO1}]$$

$$= I_{C2} = \alpha_2 I_k + I_{CBO2}$$

$$\Rightarrow \quad I_A - [\alpha_2 I_A + I_{CBO1}] = \alpha_2 I_k + I_{CBO2}$$

$$I_A - \alpha_2 I_A - \alpha_2 I_k = I_{CBO1} + I_{CBO2} \qquad \ldots(iii)$$

also $I_k = I_A + I_G$

Putting I_A in equation (iii),

$$\Rightarrow \quad I_A - \alpha_1 I_A - \alpha_2 (I_A + I_G) = I_{CBO1} + I_{CBO2}$$

$$\Rightarrow \quad I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 - \alpha_2)}$$

As I_E increases then current gain α increase due to this $I_A \uparrow$. This effect is cummulative effect, So, the anode current rieses to full load current.

Difference Between Two Transistor Mode and Thyristor

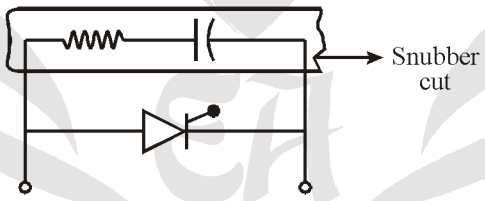
(i) The two transistor model required the continuous base current for the transistor therefore the base current not reduce to zero but in case of SCR, the gate current is reduce to zero, once the SCR is in conduction mode

(ii) In order to switch off the thyristor, a reverse voltage must be applied while in case of transistor, the base current must be reduce to zero for turning off the device.

2.5 METHOD OF TRIGGERING OF SCR

2.5.1 $\frac{dv}{dt}$ Triggering

When the rate of change of forward voltage across the thyristor is large the current $C\frac{dv}{dt}$ flows in reverse biased junction J_2. This may cross the latch current and device may be turned on. $\frac{dv}{dt}$ triggering is not preferred because the voltage transient in the circuit may causes false triggering of the device. This false triggering can be avoided by using a circuit called **snubber** circuit. Snubber circuit contains series RC circuit connected across the thyristor.



2.5.2 Forward Voltage Triggering

In this method the forward voltage is greater than V_{FB} is applied across the device. This voltage results in avalanche break down of reverse bias junction J_2 and hence the device is turn on. losses in the device is maximum during turn on process therefore, the large anode voltage in forward voltage triggering may damage the device. Hence this method of triggering is not preferred.

2.5.3 Gate Triggering

This is the most commonly used method of triggering of SCR, the injection of carriers at reversed biased junction through gate results in reduction of the forward break over voltage (V_{FB}) and thus the device can be turn on by injecting the charge carrier through gate at a particular forward voltage which is always less than the forward break over voltage V_{FB} when gate current is zero. Magnitude of gate current = 20 to 200 mA. For reducing the turn on time of SCR, the pulse of small width and large amplitude should be applied at gate terminal .The pulse width of gate current must be greater that turn on time of SCR. When the amplitude of gate pulse is large than the minimum gate current required for turning on of SCR, the device is called Hard driven or driven.

2.5.4 Light Triggering

In this method, the reversed biased junction is irradiated through a window which results in generation of electron holes pair and due to this current increases and then ultimately junction break down occurs. The *SCR employing light triggering are called LASCR (Light activated SCR). LASCR is used in HVDC transmission system.*

2.5.5 Temperature Triggering

During the forward blocking, the reverse saturation current flows through the reverse biased junction the current causes the heating which rises the temperature. Due to increase in temperature electron hole pair are generated. Which further increases the reverse saturation current and hence the heating of the junction increase and thus the effects become cummulative which ultimately results in the breakdown of reverse bias junction and the device is turned on. *Temperature triggering can damage the device due to heating so it is not used.*

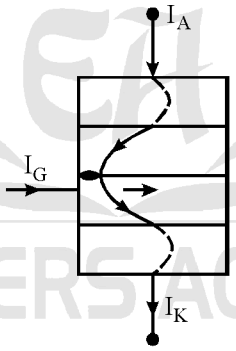
2.6 *RATING OF THYRISTOR*

2.6.1 $\frac{dv}{dt}$ rating

It is the maximum rate of change of anode voltage above which the device is turned on.

2.6.2 $\frac{di}{dt}$ rating

When the device is turned on then the current through the reverse bias junction J_2 starts flowing through the part of the junction nearest to gate and if the rate of increase in anode current is larger than the spread rate of conduction channel then more current will flow through the small area of conduction channel. This result the heat up of junction J_2 which can damage the device.



2.6.3 Surge Current Rating

This rating indicates the maximum possible non (only one time) repetitive surge current which the device can with stand without getting damage .*The surge current rating (I_s)*

$$I_s = I\sqrt{\frac{T}{t}}$$

Where, I_s = Surge current passed for time 't'.

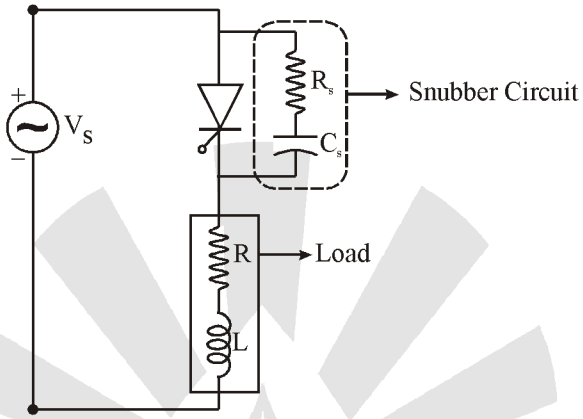
I = Surge current passed for time T

T= Half cycle of the wave.

2.7 *PROTECTION OF SCR*

2.7.1 $\frac{dv}{dt}$ Protection

When large dv/dt is applied across the thyristor under forward blocking state the current through reverse biased junction may cross the latching current which may result in false triggering of SCR. The device is protected against large dv/dt by connecting a series RC circuit known as snubber circuit across the thyristor.



$$\left.\frac{dv}{dt}\right|_{max} = \frac{V_s R_s}{L}$$

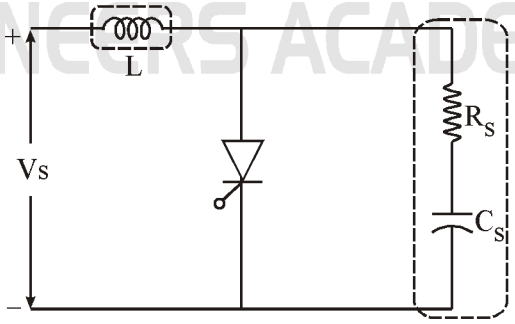
$$\left.\frac{dv}{dt}\right|_{max} = R_s\left(\frac{di}{dt}\right)_{max}$$

$$R_s = 2\xi\sqrt{\frac{L}{C_s}}$$

ξ = Damping ratio

2.7.2 $\frac{di}{dt}$ Protection

Large di/dt may cause thermal damage to the Thyristor. The device is protected against the di/dt by connecting the inductor in series with the SCR.



2.7.3 Over Voltage Protection

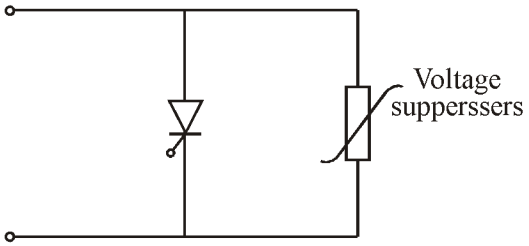
The over voltage may result in maloperation (unwanted triggering) of the device or may damage the device. The device is protected against the over voltages by connecting the voltage suppresser across the device. The voltage suppressers is a device which has negative resistance. Their resistance decreases when the voltage across them crosses some critical value. The voltage clamping devices can be :

(a) Selenium diode

(b) Metal oxide Veristor (MOV)

(c) Avalanche diode suppresser

(d) Spark gap



2.7.4 Over Current Protection

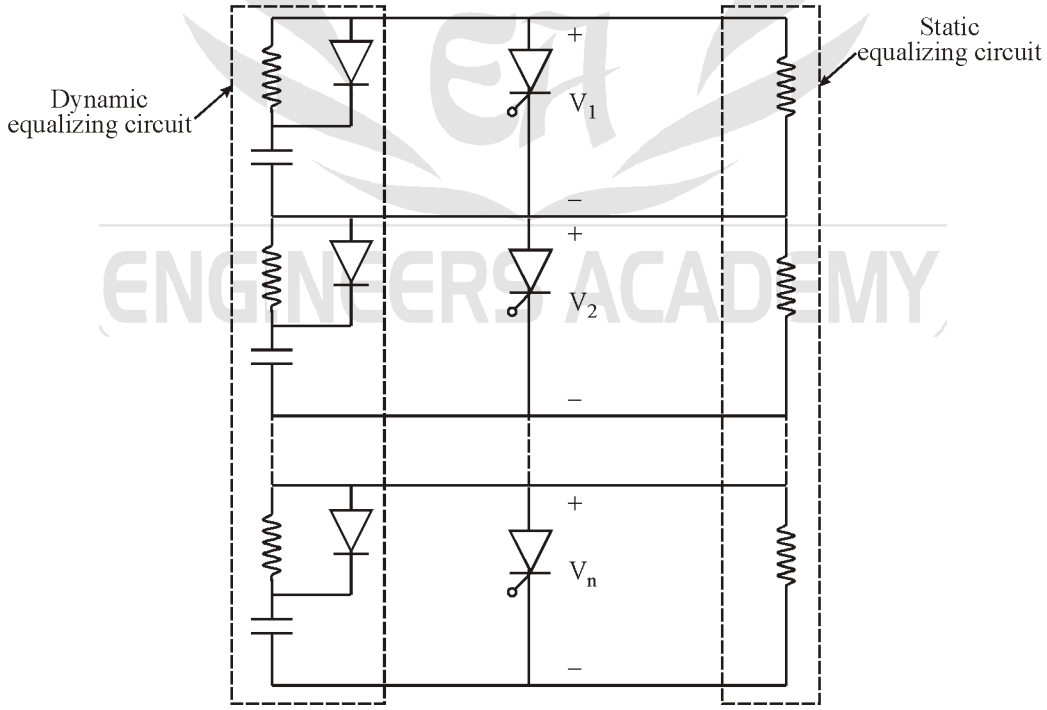
The overcurrent can flow through the device either due to short circuit or due to overloading. The protection against overloading is provided using circuit breaker (CB) and protection against short circuit can be provided using HRC fuse.

2.7.5 Gate Circuit Protection

The flux linkage of the load circuit with the gate cuircuit of different SCR can result in false triggering due to induced voltage.It can be avoided by locating SCR symmetrical on heat sink. *The heat sinks are made up of aluminium.*

2.8 *SERIES OPERATION OF SCRS*

Thyristors are connected in series to increase the overall voltage rating when the system voltage exceeds the rating of single thyristor. Voltage equalization is used to protect the thyristors during turn off by equalizing voltages across individual thyristor . The voltage should not exceed the rating of individual SCR.



Static Equalizing Circuit :

It consist of resistance connected across the thyristor. It is used to equalise the voltage across each thyristor when thyristor are in conducting state or OFF state.

Dynamic Equalizing Circuit :

This circuits used to equalise the voltage across the thyristor during dynamic condition that is during turn on and turn off process. This circuit serves the dual purpose, it equalize the voltage during dynamic condition and simultaneously it protects the device against the $\frac{dv}{dt}$.

In other word the dynamic circuit is also behaves as snubber circuit.

String Efficiency (η) :

String efficiency, $$\eta = \frac{\text{Total voltage across the string (whole system)}}{\text{(No. of SCR)} * \text{(Rating of one SCR)}}$$

$$\eta = \frac{V_s}{n \times V_{TR}}$$

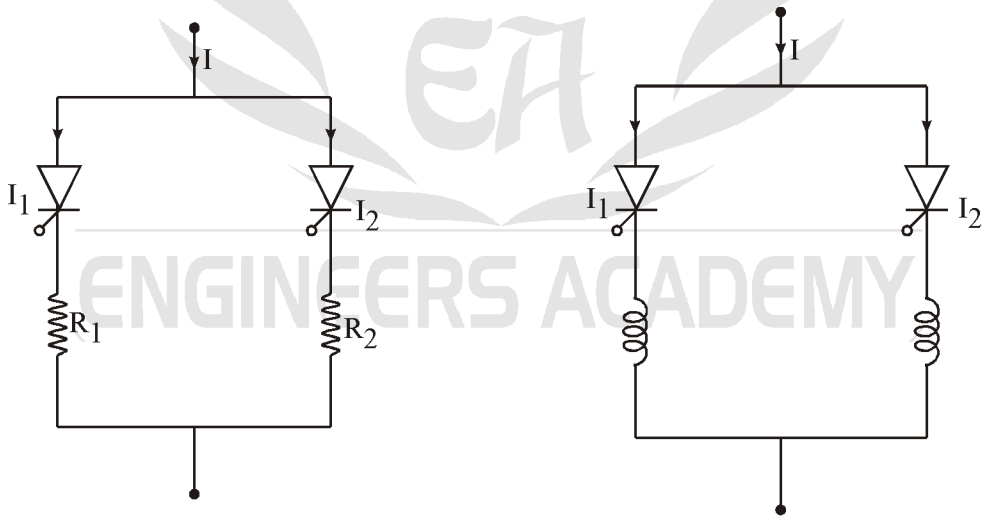
Derating factor $$DRF = 1 - \eta$$

2.9 *PARALLEL OPERATION OF SCRs*

SCRs are connected in parallel to increase over all current rating when the load current exceeds the current rating of individual SCRs. current equalization circuit is used to protect the Thyristor against very large current through a thyrister having smallest turn on time during the turn on process?

Static Equalizing Circuit

It is used to distribute the load current among the thyristor in proper to their rating. This consist of the resistances connected in series with the SCRs.



Static Equalizing Circuit *Dynamic Equilizing Circuit*

The static equalising circuit can not be used during dynamic condition because of different turn on and turn off time of SCR. The dynamic equalizing circuit is used to equalize the load current among the SCR during turn on and turn off processes, it consists of inductor connected in series with each thyristor.

The inductor connected in series with the SCR protects against the $\frac{di}{dt}$ during turn on.

2.10 *THYRISTOR COMMUTATIONS TECHNIQUES*

Commutation of thyristor is nothing but turning off thyristor. A thyristor can be turned off by using the following technique.

(a) By reducing the anode current below the holding current.

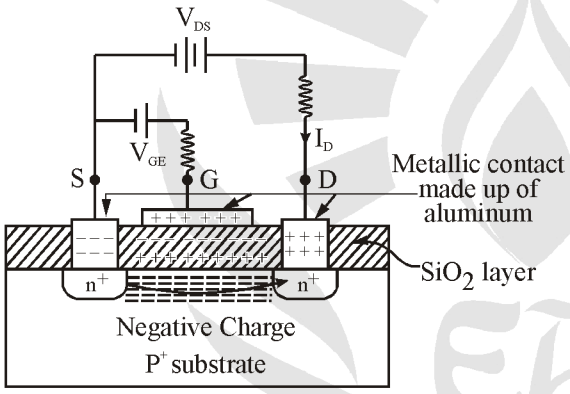
(b) By applying large impulse of voltage (in reverse direction) across the thyristor.

2.11 *POWER MOSFET*

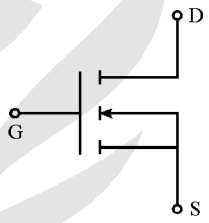
2.11.1 Basic Device Structure:

Power MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) are the most commonly used power devices due to their low gate drive power, fast switching speed and superior paralleling capability. Most power MOSFETs feature a vertical structure with Source and Drain on opposite sides of the wafer in order to support higher current and voltage.Through MOSFETs are mainly used for <200V voltage rating due to their higher channel density and thus lower on-resistance. Planar MOSFETs are good for higher voltage ratings since on-resistance is dominated by epi-layer resistance and high cell density is not beneficial. The basic MOSFET operation is the same for both structures. Unless specified, the N-channel trench MOSFET is discussed in this application note.

Layer diagram of N-channel enhancement type MOSFET



Trench MOSFET Structure



Symbol of MOSFET

Source : Terminal at which majority carrier enter into the device.

Drain : Terminal at which majority carrier leave the device.

Gate : Control input voltage is applied.

The MOSFET work in two modes called Depletion mode and enhancement mode, the Conducting channel of MOSFET can be *n*- channel and *p*-channel.

The layer diagram of enhancement mode is shown in the figure above.In enhancement mode n-channel MOSFET, source and drain layer are n^+ are defused inside the p^+ substrate shown in the diagram.

The external terminal of source and drain are mode through metallic contacts and *SiO_2 layer is used to isolate the gate from P substrate.*

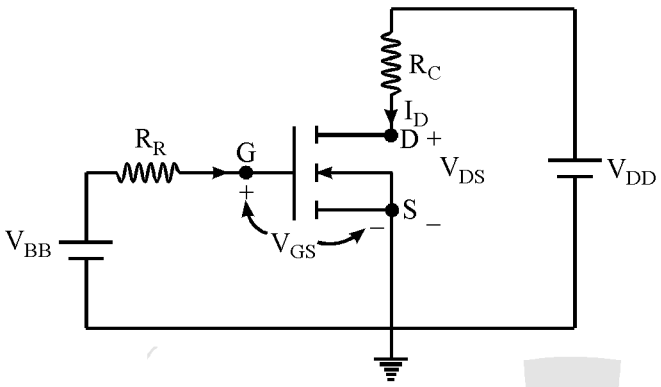
2.11.2 Working :

During enhancement mode, the drain is kept at positive potential as compare to source and a voltages V_{GS} with its positive terminal at gate is connected between gate and source due to the positive potential at gate (G), the dielectric layer (SiO_2layer) gets polarized and thus result into electrostatic field in the P substrate.

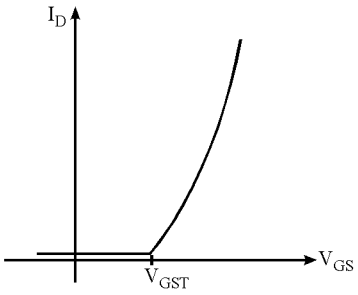
This electrostatic field results in formation of n-channel between source and drain and current start flowing from drain to source through the device.

2.11.3 Transfer Characteristic :

It is between V_{GS} and I_D



N-channel Power MOSFET circuit



Transfer characteristic

Note: *MOSFET is voltage controlled (VCCs)device and BJT is current control device (CCCs).*

For high frequency operation, MOSFET is used and UJT is used only for triggering circuit not for switching circuit..

V_{GST} = *Threshold voltage*

It is the minimum value of

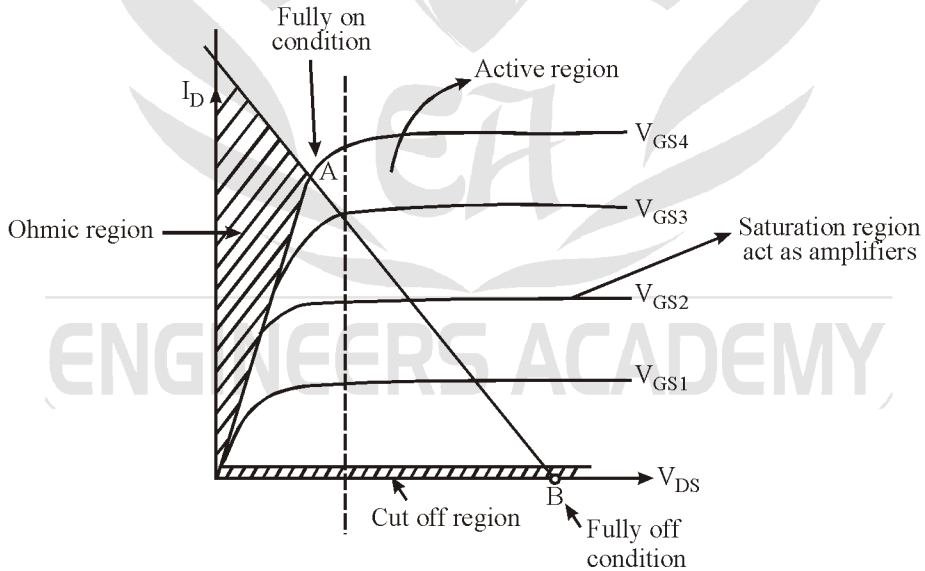
V_{GS} *required for the formation of n-channel.*

V_{GST} = 2 to 3V

2.11.4 Output Characteristics :

It is plotted between V_{DS} and I_D with V_{GS} as a parameter.

In ohmic region it works as ON, in cut-off it works as OFF



Active regions means the device is working as an amplifier.

When the MOSFET is operated in switching mode it works in either cut off or at the edge of the ohmic region.

➢ **Breakdown Voltage:**

At B, V_{DSS} is usually defined as the drain to source voltage when leakage current is 250 uA. The leakage current flowing between source and drain is denoted by I_{DSS}. The leakage current flowing between source and drain is denoted by I_{DSS}. It is measured at 100% of the B, V_{DSS} rating. As temperature increases, I_{DSS} increases and at B, V_{DSS} also increases for power MOSFETs.

PRACTICE SHEET

OBJECTIVE QUESTIONS

1. Peak inverse current and reverse recovery time depends on

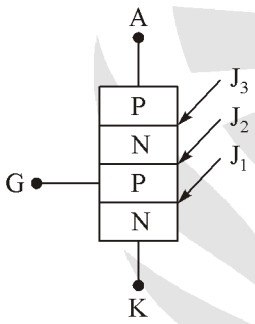
(a) Stored charge, $\frac{di}{dt}$ of forward current

(b) Stored charge

(c) $\frac{di}{dt}$ of forward current

(d) None of these

2. Figure shown a thyristor with the standard terminations of anode (A), cathode (K), gate (G) and the different junctions named J_1, J_2 and J_3. When anode to cathode voltage is positive and SCR is about to conduct load current.



(a) J_1 and J_2 are forward biased and J_3 is reverse biased.

(b) J_1 and J_3 are forward biased and J_2 is reverse biased.

(c) J_1 is forward biased and J_2 and J_3 are reverse biased.

(d) J_1, J_2 and J_3 are all forward biased.

3. The main reason for connecting a pulse transformer at a output stage of a thyristor triggering circuit is to

(a) amplify the power of the triggering pulse

(b) provide electrical isolation

(c) reduce the turn-on time of the thyristor

(d) avoid spurious triggering of the thyristor due to noise

4. Turn-on and turn-off times of transistor depend on

(a) Static characteristic

(b) Junction capacitances

(c) Current gain

(d) None of the above

5. Which one of the following statements is correct? The turn off times of converter grade SCRs are normally in the range of

(a) 1 to 2 microseconds

(b) 50 to 200 microseconds

(c) 500 to 1000 microseconds

(d) 1 to 2 milliseconds

6. Which one of the following statements is correct? For an SCR dv/dt protection is achieved through the use of

(a) RL in series with SCR

(b) RC across SCR

(c) L in series with SCR

(d) RC in series with SCR

7. In the case of a thyristor, di/dt capability can be improved by

(a) thermal triggering (b) voltage triggering

(c) dv/dt triggering (d) gate pulse triggering

8. If the amplitude of the gate pulse to thyristor is increased then

(a) both delay time and rise time would increase.

(b) the delay time would increase but the rise time would decrease.

(c) the delay time would decrease but the rise time would increase.

(d) the delay time would decrease while the rise time remains unaffected.

9. In order to obtain static voltage equalization in series-connected SCRs connections are made of
   (a) one resistor across the string
   (b) resistors of different values across each SCR
   (c) resistors of the same value across each SCR
   (d) one resistor in series with the string

10. It is preferable to use a train of pulse of high frequency for gate triggering of SCR in order to reduce
   (a) $\frac{dv}{dt}$ problem
   (b) $\frac{di}{dt}$ problem
   (c) the size of the pulse transformer
   (d) the complexity of the firing circuit

11. In a thyristor with series reactor, the firing angle of thyristor is to be controlled in the range of
   (a) 0° to 90° (b) 0° to 180°
   (c) 90° to 180° (d) 90° to 270°

12. The sharing of the voltages between thyristors operating in series is influenced by their
   (a) $\frac{di}{dt}$ capabilities
   (b) $\frac{dv}{dt}$ capabilities
   (c) junction temperatures
   (d) static v-i characteristics and leakage currents

13. Equalising circuits are provided across each SCR in series operation to provide uniform
   (a) current distribution (b) firing of SCRs
   (c) voltage distribution (d) none of the above

14. An SCR can be brought to forward conducting state with gate-circuit open when the applied voltage exceeds
   (a) the forward breakover voltage
   (b) reverse breakdown voltage
   (c) 1.5V
   (d) none of these

15. Turn-on time of an SCR can be reduced by using a
   (a) rectangular pulse of high amplitude and narrow width
   (b) rectangular pulse of low amplitude and wide width
   (c) triangular pulse
   (d) trapezoidal pulse

16. A forward voltage can be applied to an SCR after its
   (a) anode current reduces to zero
   (b) gate recovery time
   (c) reverse recovery time
   (d) anode voltage reduces to zero

17. A triac is a
   (a) 2 terminal switch
   (b) 2 terminal bilateral switch
   (c) 3 terminal unilateral switch
   (d) 3 terminal bidirectional switch

18. A resistor connected across the gate and cathode of an SCR
   (a) increases $\frac{dv}{dt}$ rating of SCR
   (b) increases holding current of SCR
   (c) increases noise immunity of SCR
   (d) increases turn-off time of SCR

19. Once SCR starts conducting a forward current its gate loses control over
   (a) anode circuit voltage only.
   (b) anode circuit current only.
   (c) anode circuit voltage and current
   (d) anode circuit voltage, current and time.

20. The turn-off time is longer than the turn-on time in SCR because

(a) The anode and cathode functions get reverse biased while gate junctions is still forward biased.

(b) the forward break-over voltage is high.

(c) the gate pulse has been removed.

(d) none of these.

21. In an UJT, with V_{BB} as the voltage across two base terminals, the emitter potential at peak point is given by

(a) ηV_{BB} (b) ηV_D

(c) $\eta V_{BB} + V_D$ (d) $\eta V_D + V_{BB}$

22. When an UJT is used for triggering an SCR, the wave shape of the voltage obtained from UJT circuit is a

(a) sine wave (b) saw-tooth wave

(c) trapezoidal wave (d) square wave

23. Which of the following statements are correct when a positive voltage is applied to the gate of a reverse biased SCR?

1. This injectes more electrons into junction J_v

2. This increases reverse leakage current into anode.

3. Heating of junction is unaffected.

4. Failure of junction occurs due to thermal runaway,

(a) 1 and 3 (b) 1 and 4

(c) 2 and 3 (d) 2 and 4

24. Match List I (Devices) with List II (Properties) and select the correct answer using the codes given below the lists:

List-I

A. TRIAC

B. Reverse conducting thyristor (RCT)

C. Gate turn-off thyristor(GTO)

D. Amplifying gate thyristor

List – II

1. Good di/dt behaviour even at low gate currents

2. Normally provided with a small continuous negative gate pulse during off state

3. Negative gate pulse for reverse conduction

4. No gate pulse for reverse conduction

Codes:	A	B	C	D
(a)	4	3	1	2
(b)	3	4	2	1
(c)	3	4	1	2
(d)	4	3	2	1

25. When compared to those asymmetrical thyristor, the turn-off time and reverse blocking voltage of an asymmetrical thyristor respectively

(a) large and large (b) large and small

(c) small and large (d) small and small

26. Which of the following characteristics are possessed by IGBT

1. High input impedance

2. Secondary discharge problem

3. Current controlled device

4. Low switching loss

5. Faster than BJT

(a) 1,4 and 5 (b) 1,2 and 4

(c) 2, 3 and 5 (d) 1,3 and 5

27. The correct sequence of the following devices in the increasing order of turn-off times is

(a) MOSFET, IGBT, BJT, Thyristor

(b) IGBT, MOSFET, BJT, Thyristor

(c) Thyristor, BJT, MOSFET, IGBT

(d) MOSFET, BJT, IGBT, Thyristor

28. The correct sequence of given devices in the decreasing order of their speeds of operation is

(a) power BJT, power MOSFET, IGBT, SCR

(b) IGBT, power MOSFET power BJT, SCR

(c) SCR, power BJT, IGBT, power MOSFET

(d) power MOSFET, IGBT, power BJT, SCR